GENERAL DESCRIPTION

The MX5114 is designed to drive low-side MOSFETs in boost-type configurations or to drive secondary synchronous MOSFETs in isolated topologies. With strong sink current capability, the MX5114 can drive. multiple FETs in parallel. The MX5114 also has the features necessary to drive low-side enhancement mode Gallium Nitride (GaN) FETs. The MX5114 provides inverting and noninverting inputs to satisfy requirements for inverting and Noninverting gate drive in a single device type. The inputs of the MX5114 are TTL/CMOS Logic compatible and withstand input voltages up to 14 V regardless of the VDD voltage. The MX5114 has split gate outputs, providing flexibility to adjust the turnon and turnoff strength independently. The MX5114 has fast switching speed and minimized propagation delays, facilitating high-frequency operation. The MX5114 is available in a 6-pin SOT-23 package and a 6-pin WSON package with an exposed pad to aid thermal dissipation.

FEATURES

- ♦ Independent Source and Sink Outputs for Controllable Rise and Fall Times
- ♦ 4-V to 12.6-V Single Power Supply
- ♦ 7.6-A/1.3-A Peak Sink and Source Drive Current
- ♦ 0.23-Ω Open-drain Pulldown Sink Output
- ♦ 2-Ω Open-drain Pullup Source Output
- ♦ 12-ns (Typical) Propagation Delay
- ♦ Matching Delay Time Between Inverting and Noninverting Inputs
- ♦ TTL/CMOS Logic Inputs
- ♦ 0.68-V Input Hysteresis
- ♦ Up to 14-V Logic Inputs (Regardless of VDD Voltage)
- ♦Low Input Capacitance: 2.5-pF (Typical)
- ♦–40°C to 125°C Operating Temperature Range
- ♦ 6-Pin SOT-23

APPLICATIONS

Boost Converters

Flyback and Forward Converters

Secondary Synchronous FETs Drive in Isolated Topologies

These are Pb-free device

Motor Control

GENERAL INFORMATION

Ordering information

Part Number	Description
MX5114A	CMOS
MX5114B	TTL

Package dissipation rating

Package	RθJA（°C/W）
SOT-23 (6)	108.1
WSON (6)	51.0

Absolute maximum ratings

Parameter	Value
VDD to VSS	-0.3 to 14V
IN, INB to VSS	-0.3 to 14V
N_OUT to VSS	-0.3 to VCC+0.3V
P_OUT to VSS	-2.0 to VCC+0.3V
Junction temperature	150℃
Storage temperature, Tstg	-55 to 150℃

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended operating condition

Symbol	Parameter	Range
VDD	VCC supply voltage	4-12.6V
Junction temperature		40-125℃

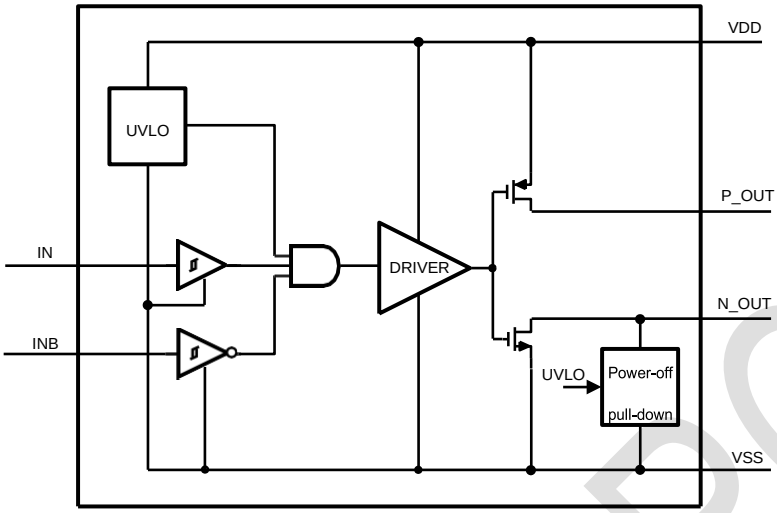


Figure 1 MX5114 Block Diagram

TERMINAL ASSIGMENTS

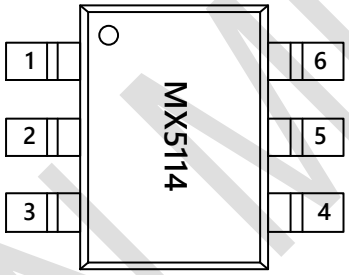


Figure 2 pin information

PIN NO.	PIN name	Description
1	ENA	Enable input for channel A. A logic high enables channel A (the state of OUTA is determined by INA). A logic low disables OUTA (OUTA held low regardless of INA). Floating is logic high internal.
2	INA	Channel A logic input. Internally pulled to GND.
3	GND	Ground. Common ground reference for the device.
4	INB	Channel B logic input. Internally pulled to GND.
5	OUTB	Channel B output, capable of sourcing and sinking 5A
6	VCC	Supply voltage.
7	OUTA	Channel A output, capable of sourcing and sinking 5A
8	ENB	Enable input for channel B. A logic high enables channel B (the state of OUTB is determined by INB). A logic low disables OUTB (OUTB held low regardless of INB). Floating is logic high internal.
The thermal pad on the bottom of the thermally enhanced device, MX27524ES, may be connected to GND or left floating; it must not be connected to any other net. The thermal pad is not intended to carry current.		

BLOCK DIAGRAM

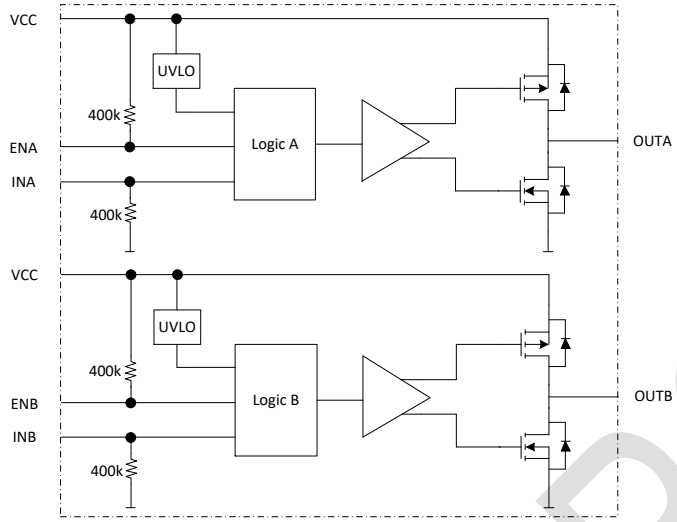


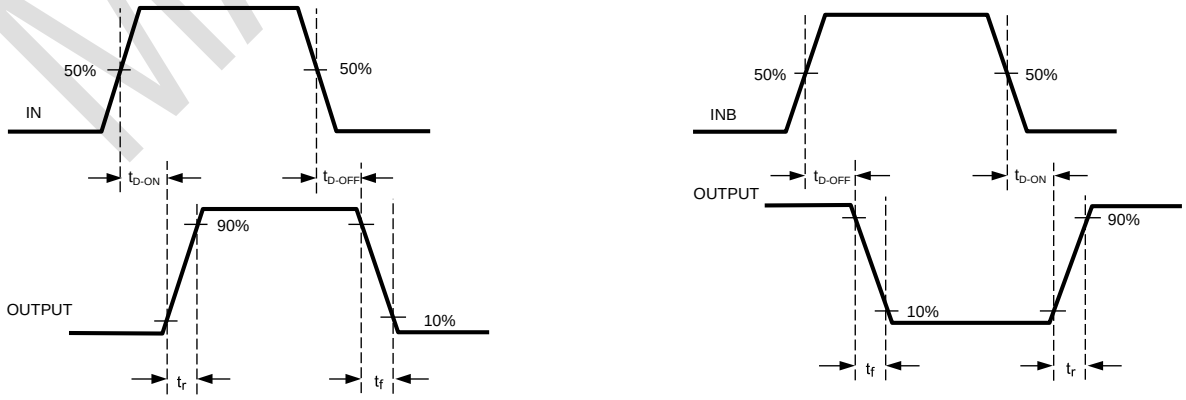
Figure 3 block diagram

Electrical characteristics

（TA=25°C， VCC=12V, unless otherwise noted）

Symbol	Parameter	Test condition		Min	Typ.	Max	Unit
POWER SUPPLY							
VDD	VDD operating voltage		(TJ) range of –40°C to 125°C	4.0		12.6	V
UVLO	VDD undervoltage lockout	VDD Rising	TJ = 25°C		3.6		V
			(TJ) range of –40°C to 125°C	3.25		4.00	
	VDD undervoltage lockout hysteresis				0.4		V
IDD	VDD quiescent current	IN = INB = VDD	TJ = 25°C		0.95		mA
			(TJ) range of –40°C to 125°C			1.9	
	N-CHANNEL OUTPUT						
RON-N (SOT-23-6)	Driver output resistance – pulling down	VDD = 10 V, I_{N-OUT} = –100 mA	TJ = 25°C		0.23	0.26	Ω
			TJ = 125°C		0.38	0.43	Ω
		VDD = 4.5 V, I_{N-OUT} = –100 mA	TJ = 25°C		0.24	0.28	Ω
			TJ = 125°C		0.40	0.47	Ω
RON-N (WSON-6)	Driver output resistance – pulling down	VDD = 10 V, I_{N-OUT} = –100 mA	TJ = 25°C		0.31	0.34	Ω
			TJ = 125°C		0.46	0.51	Ω
		VDD = 4.5 V, I_{N-OUT} = –100 mA	TJ = 25°C		0.32	0.36	Ω
			TJ = 125°C		0.48	0.55	Ω
	Power-off pulldown resistance	VDD = 0 V, I_{N-OUT} = –10 mA			3.3	10	Ω
	Power-off pulldown clamp voltage	VDD = 0 V, I_{N-OUT} = –10 mA			0.85	1.0	V
ILK-N	Output leakage current	N_OUT = VDD	TJ = 25°C		6.85		µA
			(TJ) range of –40°C to 125°C			20	

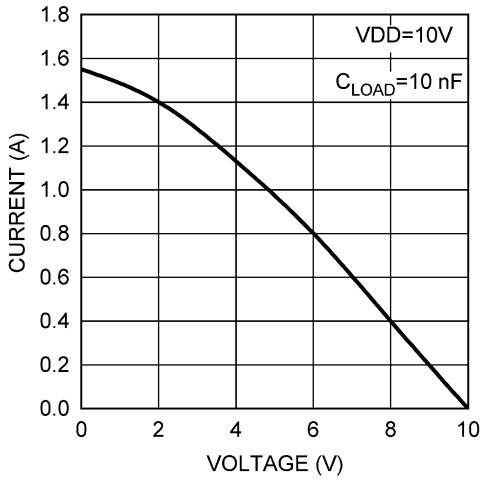
IPK-N	Peak sink current	C_L = 10,000 pF	T_J = 25°C		7.6		A
	P-CHANNEL OUTPUT						
R_{ON-P} (SOT-23-6)	Driver output resistance – pulling up	VDD = 10 V, I_{P_OUT} = 50 mA	T_J = 25°C		2.00	3.00	Ω
			T_J = 125°C		2.85	4.30	Ω
		VDD = 4.5 V, I_{P_OUT} = 50 mA	T_J = 25°C		2.20	3.30	Ω
			T_J = 125°C		3.10	4.70	Ω
R_{ON-P} (WSON-6)	Driver output resistance – pulling up	VDD = 10 V, I_{P_OUT} = 50 mA	T_J = 25°C		2.08	3.08	Ω
			T_J = 125°C		2.93	4.38	Ω
		VDD = 4.5 V, I_{P_OUT} = 50 mA	T_J = 25°C		2.28	3.38	Ω
			T_J = 125°C		3.18	4.78	Ω
ILK-N	Output leakage current	P_OUT = 0	T_J = 25°C		0.001		µA
			(T_J) range of –40°C to 125°C			10	
IPK-N	Peak sink current	C_L = 10,000 pF	T_J = 25°C		1.3		A
	LOGIC INPUT						
V_{IH}	Logic 1 input voltage	MX5114A	(T_J) range of –40°C to 125°C	0.67 × VDD			V
		MX5114B		2.4			V
V_{IL}	Logic 0 input voltage	MX5114A	(T_J) range of –40°C to 125°C			0.33 × VDD	V
		MX5114B				0.8	V
V_{HYS}	Logic-input hysteresis	MX5114A			1.6		V
		MX5114B			0.68		V
	Logic-input current	INB = VDD or 0	T_J = 25°C		0.001		
			(T_J) range of –40°C to 125°C			10	µA
C_{IN}	Input capacitance	2.5	F		2.5		pF

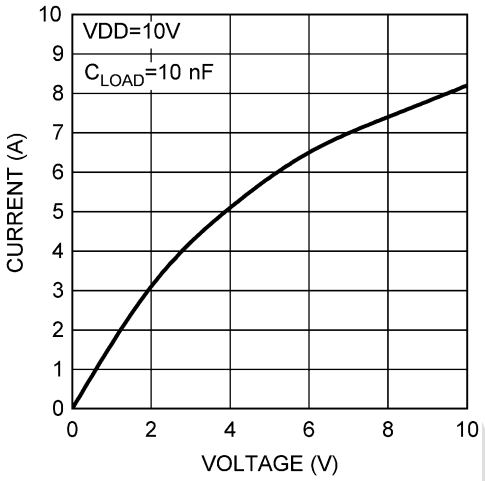


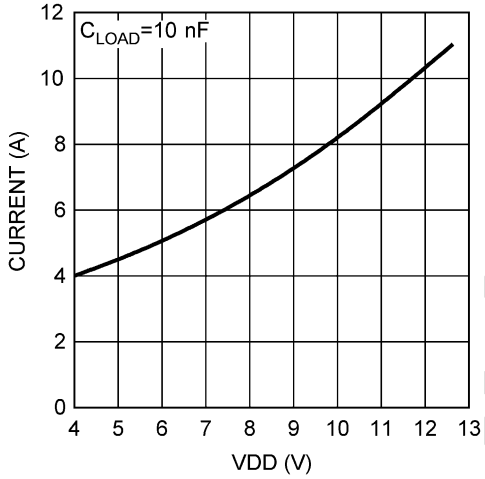
Note:P_OUT and N_OUT are tied together.

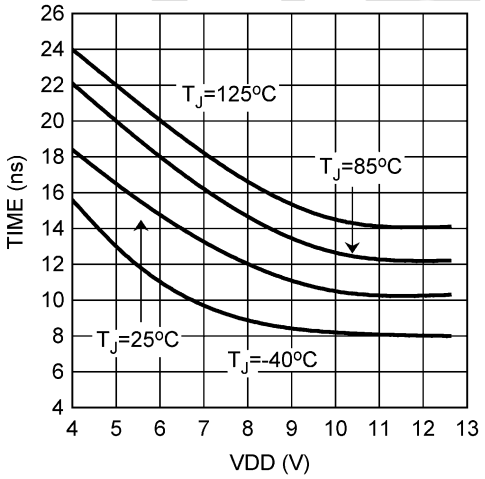
Figure 4 Timing Diagram

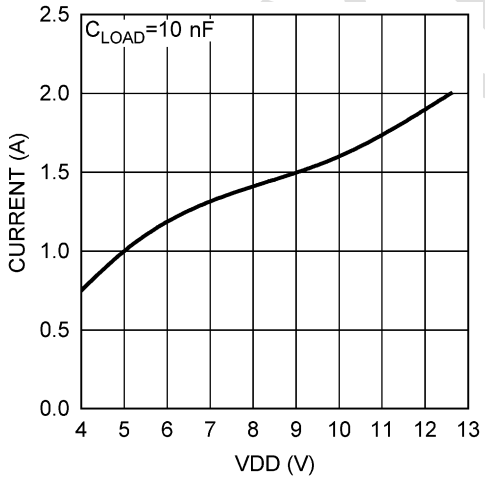
Characteristic plots

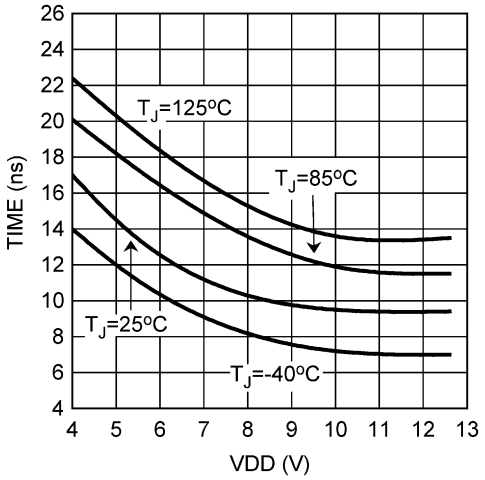


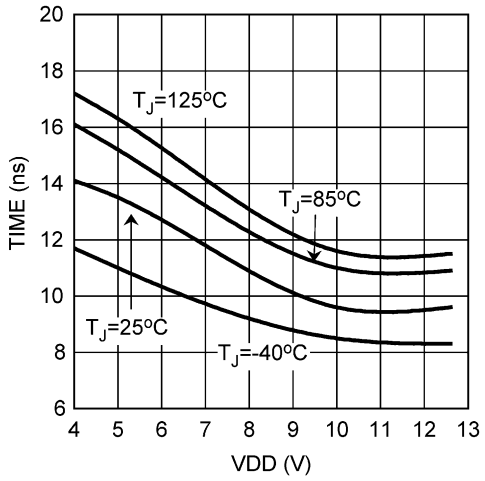


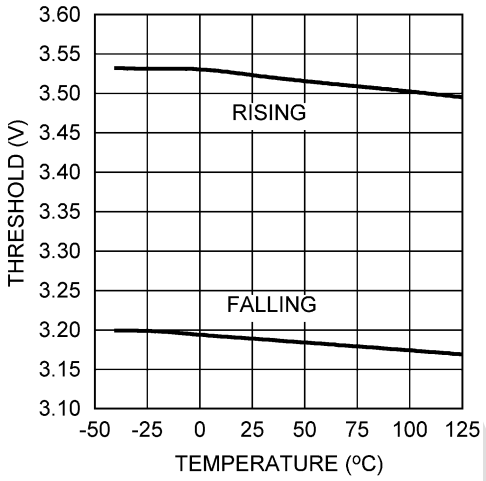


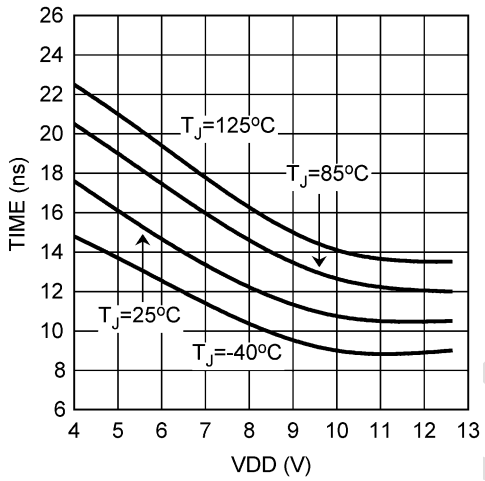


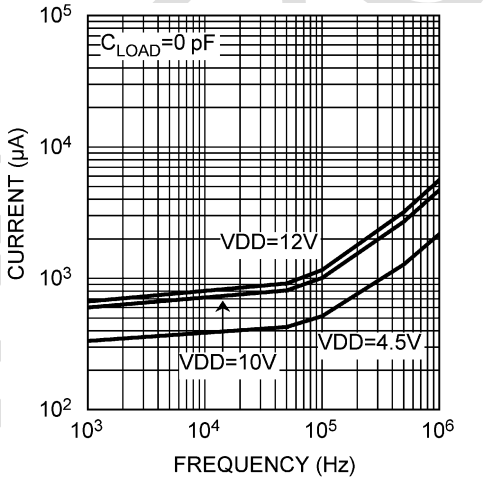


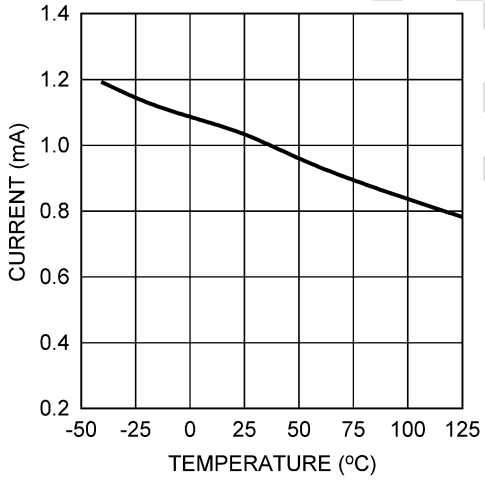


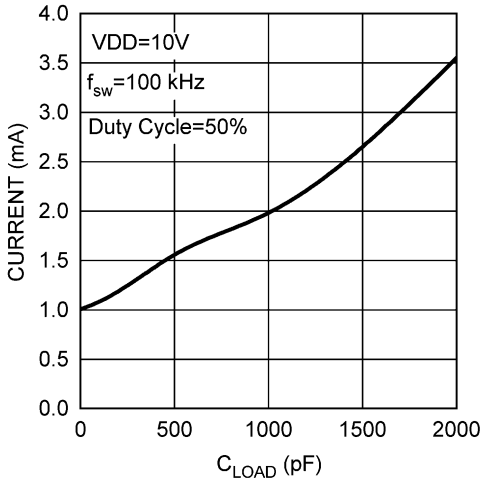

TIME (ns)
VDD (V)
T_J=125°C
T_J=85°C
T_J=25°C
T_J=-40°C

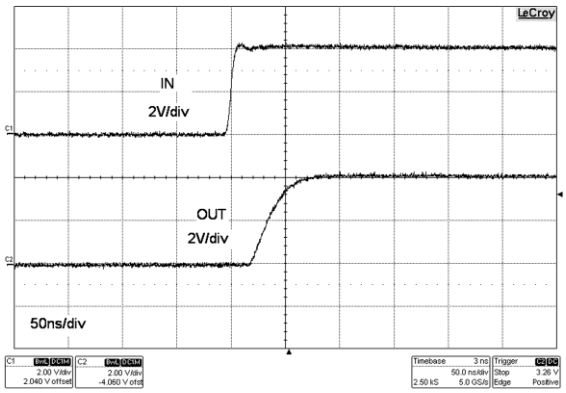

THRESHOLD (V)
TEMPERATURE (°C)
RISING
FALLING

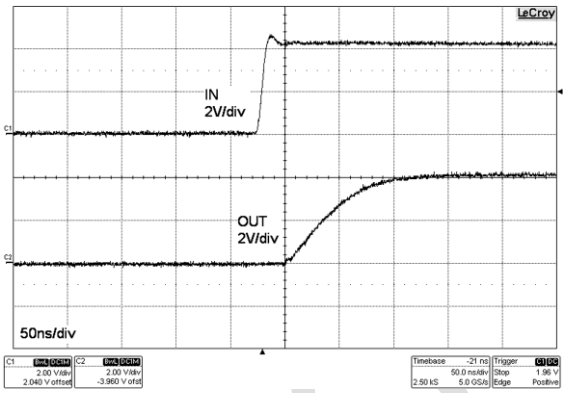

TIME (ns)
VDD (V)
T_J=125°C
T_J=85°C
T_J=25°C
T_J=-40°C

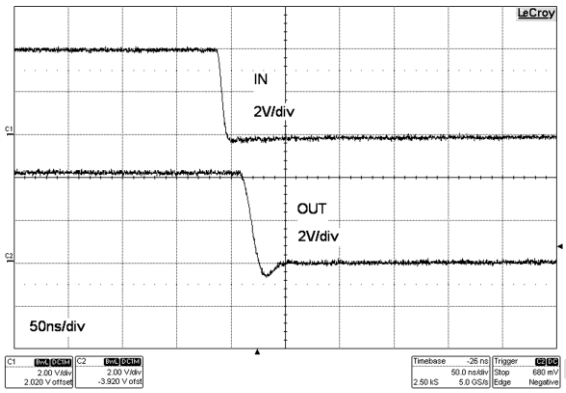

CURRENT (µA)
FREQUENCY (Hz)
C_LOAD=0 pF
VDD=12V
VDD=4.5V
VDD=10V

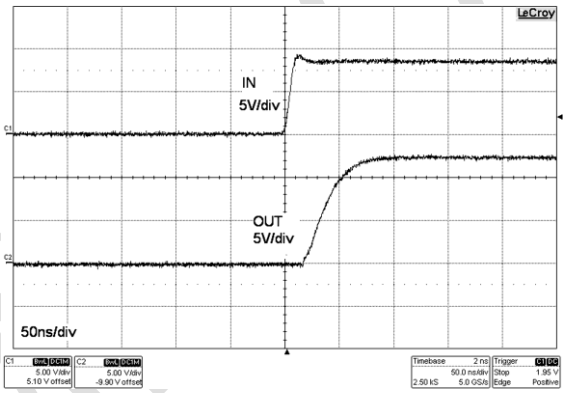

CURRENT (mA)
TEMPERATURE (°C)

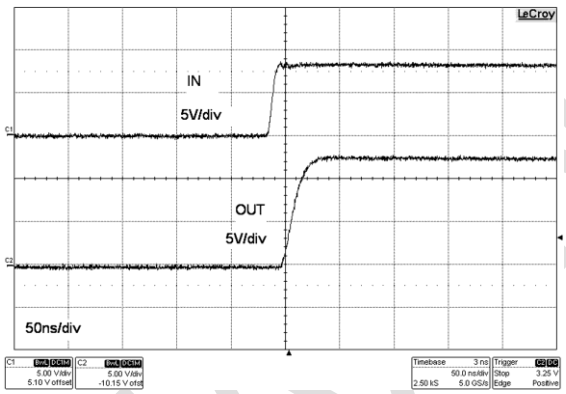

CURRENT (mA)
C_LOAD (pF)
VDD=10V
f_sw=100 kHz
Duty Cycle=50%

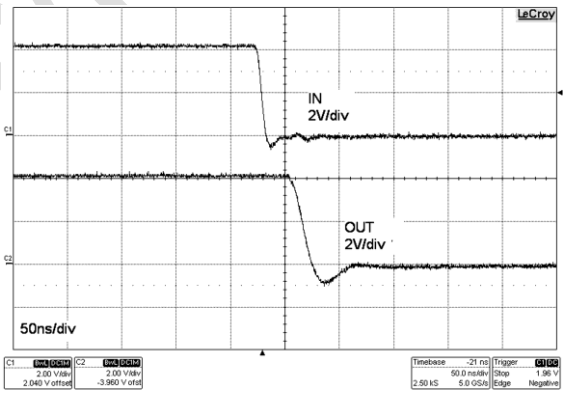

LeCroy
IN
2V/div
OUT
2V/div
50ns/div

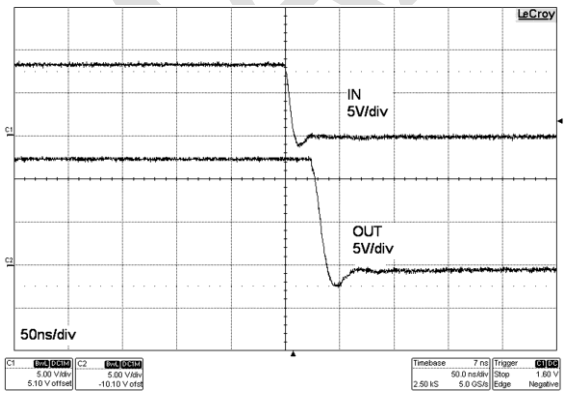

LeCroy
IN
2V/div
OUT
2V/div
50ns/div

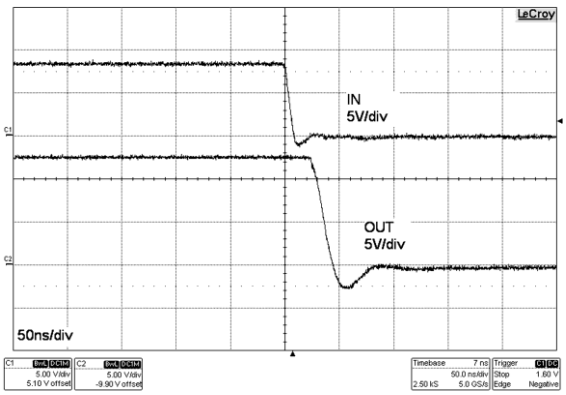

LeCroy
IN
2V/div
OUT
2V/div
50ns/div


LeCroy
IN
5V/div
OUT
5V/div
50ns/div


LeCroy
IN
5V/div
OUT
5V/div
50ns/div


LeCroy
IN
2V/div
OUT
2V/div
50ns/div


LeCroy
IN
5V/div
OUT
5V/div
50ns/div


LeCroy
IN
5V/div
OUT
5V/div
50ns/div

Operation description

The MX5114 is a single low-side gate driver with 7.6-A/1.3-A peak sink/source drive current capability. Inputs of the MX5114 are TTL Logic compatible and can withstand the input voltages up to 14-V regardless of the VDD voltage. This allows inputs of the MX5114 to be connected directly to most PWM controllers. The split outputs of the MX5114 offer flexibility to adjust the turnon and turnoff speed independently by adding additional impedance in either the turnon path or the turnoff path.

The MX5114 includes an under-voltage lockout (UVLO) circuit. When the VDD voltage is below the UVLO threshold voltage, the IN and INB inputs are ignored, and if there is sufficient VDD voltage, the output NMOS is turned on to pull the N_OUT low. In addition, the MX5114 has an internal PNP transistor in parallel with the output NMOS. Under the UVLO condition, the PNP transistor will be on and clamp the N_OUT voltage below 1 V.

Under the UVLO condition, the PNP transistor will be on and clamp the N_OUT voltage below 1 V. This feature ensures the N_OUT remaining low when VDD voltage is not sufficient to enhance the output NMOS. The MX5114 has the features necessary to drive low-side enhancement mode GaN FETs. Due to the fast switching speed and relatively low gate voltage of enhancement mode GaN FETs, PCB layout is crucial to achieve reliable operation. Refer to Layout for details.

Device Functional Modes

Table 1. Truth Table

IN	INB	P_OUT	N_OUT
L	L	OPEN	L
L	H	OPEN	L
H	L	H	OPEN
H	H	OPEN	L

Application Information

The MX5114 has the features necessary to drive low-side enhancement mode GaN FETs. Due to the fast switching speed and relatively low gate voltage of enhancement mode GaN FETs, PCB layout is crucial to achieve reliable operation.

Typical Application

Boost DC-DC converter using a 100-V enhancement mode GaN FET (EPC2001) as the boost power switch. The control circuitry is implemented with the MX5114, a 100-V current mode PWM controller.

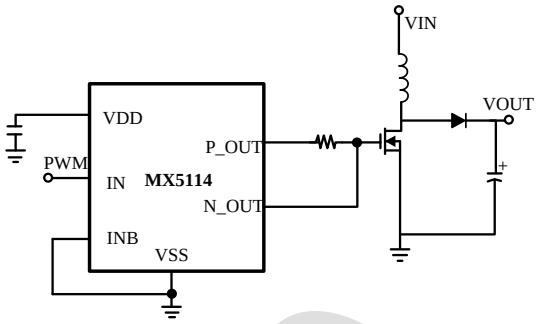


Figure 5 Simplified Boost Converter

Design Requirements

See Table 2 for the parameter and values.

PARAMETER	VALUE
Input Operating Voltage	24 V to 66 V
Output Voltage	75 V
Output Current	2 A
Measured Efficiency	97% @ at 48 V 2 A
Frequency of Operation	500 kHz

Power Dissipation

It is important to keep the power consumption of the driver below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation of the MX5114 is the sum of the gate charge losses and the losses in the driver due to the internal CMOS stages used to buffer the output as well as the power losses associated with the quiescent current.

The gate charge losses can be calculated with the total input gate charge as in Equation 1 and Equation 2:

$$P_g = Q_g \times V_{DD} \times F_{sw} \quad (1)$$

or

$$P_g = C_{LOAD} \times V_{DD}^2 \times F_{SW} \quad (2)$$

Where,Fsw is switching frequency.

The power dissipation associated with the internal circuit operation of the driver can be estimated with the characterization curves of the MX5114. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as Equation 3:

$$P = \frac{\left(T_J - T_A \right)}{\theta_{JA}} \quad (3)$$

Where ,P is the total power dissipation of the driver.

This power PG is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off.

Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

Gate Drive

The enhancement mode GaN FETs have small gate capacitance and low threshold gate voltage. Therefore GaN FETs are prone to gate oscillations induced by PCB parasitic elements. It is necessary to place the driver as close to the GaN FET as possible to minimize the stray inductance. Gate resistors can be used to damp the oscillations and to adjust the switching speed. The MX5114 has split outputs, providing flexibility to adjust the turnon and turnoff strength independently. In the evaluation board, 1.5Ω and 2.7Ω gate resistors are used in the turnon and turnoff path respectively.

Detailed Design Procedure

The MX5114 has the features necessary to drive low-side enhancement mode GaN FETs. Due to the fast switching speed and relatively low gate voltage of enhancement mode GaN FETs, PCB layout is crucial to achieve reliable operation.

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power switch. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power FET (such as dVDS/dt).

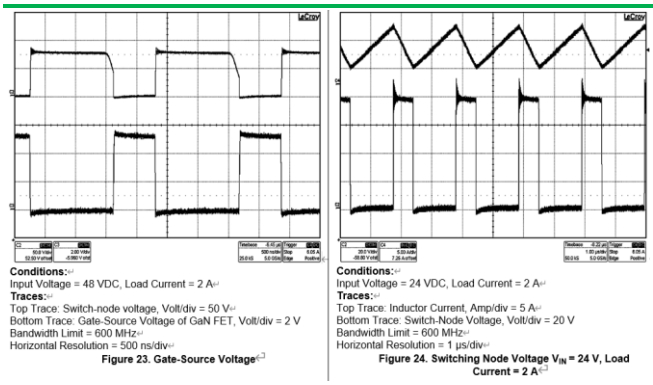
For example, the system requirement in this application might state that a EPC2001 GaN FET must be turned on with a dVDS/dt of 20 V/ns or higher with a DC bus voltage of 75 V. This requirement means that the entire drain-to-source voltage swing during the FET turnon event (from 75 V in the OFF state to VDS(on) in on state) must be completed in approximately 3.75 ns or less. When the drain-to- source voltage swing occurs, the Miller charge of the power FET (QGD parameter in EPC2001 data sheet is

2.2 nC typical) is supplied by the peak current of gate driver. To achieve the targeted dVDS/dt, the gate driver must be capable of providing the QGD charge in 3.75 ns or less. In other words a peak current of 0.586 A (=2.2 nC/2ns) or higher must be provided by the gate driver.

The MX5114 gate driver is capable of providing 1.3A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 2.2x overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the FET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × IPEAK × time) would equal the total gate charge of the power FET (QG parameter in the EPC2001 GaN FET datasheet = 8 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the GaN FET switching. In other words the time parameter in the equation would dominate and the IPEAK value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered.

Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power FET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

Application Curves



System Examples

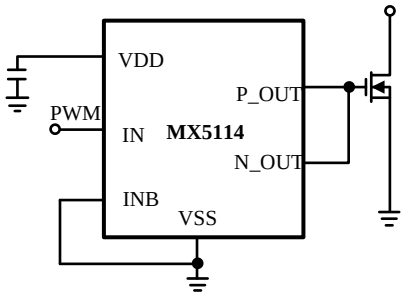


Figure 6 Noninverting Application

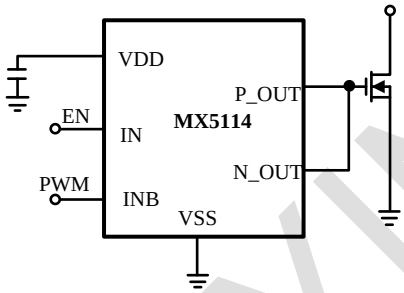


Figure 7 Inverting Application

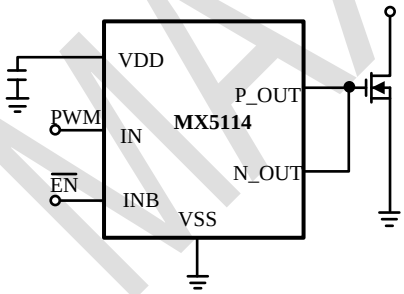


Figure 8 Noninverting Application With Enable Pin

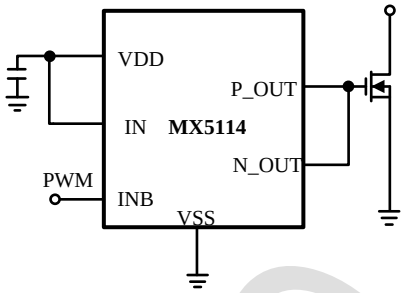


Figure 9 inverting Application With Enable Pin

Power Supply Recommendations

A low-ESR/ESL ceramic capacitor must be connected close to the IC, between VDD and VSS pins to support the high peak current being drawn from VDD during turnon of the FETs. It is most desirable to place the VDD decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.

Layout considerations

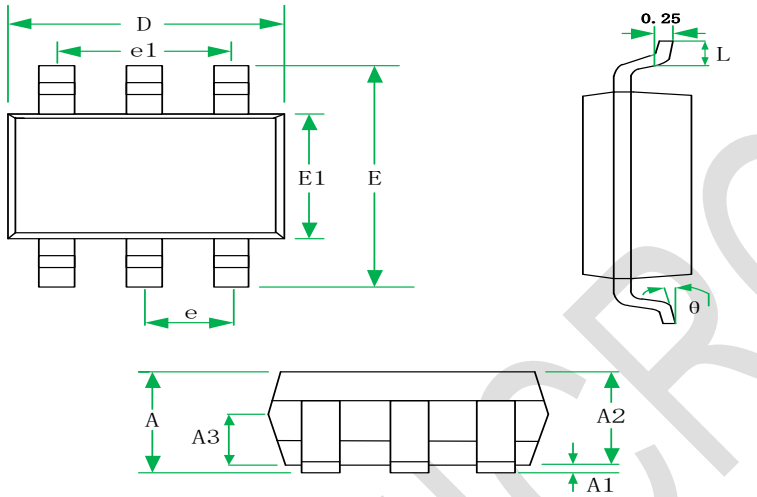
Attention must be given to board layout when using MX5114. Some important considerations include the following:

The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the FETs gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate.

To reduce the loop inductance, the driver should be placed as close as possible to the FETs. The gate trace to and from the FETs are recommended to be placed closely side by side, or directly on top of one another.

The parasitic source inductance, along with the gate capacitor and the driver pulldown path, can form a LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.

Package information



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A						
A1	0.04		0.15	0.0016		0.0059
A2	1.00	1.10	1.20	0.039	0.043	0.047
A3	0.55	0.65	0.75	0.022	0.026	0.029
D	2.72	2.92	3.12	0.107	0.115	0.123
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95BSC			0.037BSC		
e1	1.90BSC			0.074BSC		
L	0.30		0.60	0.012		0.024
θ	0		8°	0		8°

SOT23-6 for MX1210

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